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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Nicolai Kosche et al.

Title: TECHNIQUE FOR ASSOCIATING INSTRUCTIONS WITH EXECUTION EVENTS

Application No.:	10/050,358	Filed:	January 16, 2002
Examiner:	Wei Y. Zhen	Group Art Unit:	2183
Atty. Docket No.:	004-7047		

April 10, 2003

COMMISSIONER FOR PATENTS
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT UNDER *37 C.F.R. § 1.97*

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the undersigned brings the patents, publications, applications or other information identified in the attached:

☒ Form(s) PTO-1449
☒ Other: List of pending U.S. Patent Applications

to the Examiner's attention in the above-identified application. Citation of such information shall not be construed as:

1. an admission that the information necessarily is, or corresponds to, prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described below; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

FEE AUTHORIZATION

☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.

☒ The undersigned believes that this Information Disclosure Statement is being filed before the mailing date of a first Office action on the merits or before the mailing date of a first Office action after the filing of a request for continued examination under § 1.114. Therefore, no fee is believed required.

If however, this Information Disclosure Statement is filed after the period specified in § 1.97(b), the undersigned hereby authorizes the Commissioner to charge the fee set forth in § 1.17(p) to Deposit Account No. 50-0631.

CERTIFICATE OF MAILING

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231.

David W. O'Brien — 4/10/03 (Date)

Respectfully submitted,

David W. O'Brien, Reg. No. 40,107
Attorney for Applicant(s)
(512) 347-9030
(512) 347-9031 (fax)

U.S. Department of Commerce, Patent and Trademark Office	Attorney Docket No.:	004-7047
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s):	Nicolai Kosche et al.
(Use several sheets if necessary)	Filing Date:	January 16, 2002
	Group Art Unit:	2183
	Date Submitted:	April 10, 2003

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name
	1.	6,427,235	July 30, 2002	Kosche et al.

Foreign Patent Documents

					Translation	
		Document	Date	Country	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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LIST OF PENDING U.S. PATENT APPLICATIONS

The following pending U.S. patent applications are listed for consideration by the Examiner.

1) U.S. Patent Application 09/436,464 filed November 8, 1999, entitled "A Method and Apparatus for Inserting Data Prefetch Operations Using Data Flow Analysis," naming inventor Peter C. Damron (Atty Ref. P4373).

2) U.S. Patent Application 09/535,930 filed March 24, 2000, entitled "Modulo Scheduling Via Binary Search for Minimum Acceptable Initiation Interval Method and Apparatus," naming inventor Brian E. Bliss (Atty Ref. P4678).

3) U.S. Patent Application 09/594,430 filed June 15, 2000, entitled "Compiler-Based Cache Line Optimization," naming inventor Nicolai Kosche (Atty Ref. P5010).

4) U.S. Patent Application 09/630,052 filed August 1, 2000, entitled "Method and Apparatus for Software Prefetching Using Non-Faulting Loads," naming inventors Peter Damron and Nicolai Kosche (Atty Ref. P4955).

5) U.S. Patent Application 09/679,431 filed October 3, 2000, entitled "System and Method for Scheduling Memory Instructions to Provide Adequate Prefetch Latency," naming inventors Nicolai Kosche, Peter C. Damron, Joseph Chamdani and Partha Tirumalai (Atty Ref. P5370).

6) U.S. Patent Application 09/679,433 filed October 3, 2000, entitled "System and Method for Insertion of Prefetch Instructions by a Compiler," naming inventors Peter C. Damron and Nicolai Kosche (Atty Ref. P5392).

7) U.S. Patent Application 09/679,434 filed October 3, 2000, entitled "System and Method for Scheduling Instructions to Maximize Outstanding Prefetches and Loads," naming inventors Peter C. Damron and Nicolai Kosche (Atty Ref. P5369).

8) U.S. Patent Application 09/685,431 filed October 10, 2000, entitled "Heuristic for Identifying Loads Guaranteed to Hit in Processor Cache," naming inventors Nicolai Kosche and Peter C. Damron (Atty Ref. P5371).

Applicant(s) are providing a separate list of pending applications, pursuant to MPEP § 609(D), to avoid publication of the application numbers on any patent that issues from the above-identified application. Applicant(s) request that the Examiner indicate consideration of the pending applications listed above in accordance with MPEP 609(C)(2) and return a copy of this page with the next communication.